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10/042,080	01/07/2002	Robert Walter Berry JR.	AUS920010801US1	6558

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,080	BERRY ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 10/18/2004

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☒ Claim(s) 7,10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendment of 10/18/2004.

Claims 1,5-7, 10 and 11 have been amended.

Claims 1-11 are pending.

Response to Amendment

1. In view of the applicant's amendment to Claim 10, the examiner withdraws the rejection to said claim under 35 USC 112 second paragraph.

2. Also, in view of the amendments to Claims 6, 7 and 10, the examiner has found additional new grounds for rejections under 35 USC 112 second paragraph, and also new objections due to minor informalities (see below).

Response to Arguments

3. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new grounds of rejection (see below).

Claim Objections

4. Claims 7 and 10 are objected to because of the following informalities:

As per Claim 7:

The phrases "an inverted bit", and "a second SRL" (lines 1 and 2 of claim) both refer to an antecedent in Claim 6, and therefore should be changed to recite, "the inverted bit", and "the second SRL".

As per Claim 10:

The phrase "a second SRL" in line 4 of the claim implies that there is a first SRL, but no such first SRL exists in this claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. Claims 6, 7, 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per Claim 6:

The step beginning at line 6 is in contradiction with the step at line 11. Each of the two steps call for transmitting both "the first scan data bit" and "the inverted bit of the first scan data bit" to the same second SRL if there is not the logic 1 signal. Transmission of both signals using the same logic is impossible and so is indefinite. One or the other step must use a different logic signal (0 perhaps, as indicated in the Disclosure), but the examiner will rely on the applicant to change one or the other so that they do not contradict.

The phrase "logic 1 signal" in lines 7 and 12 is indefinite in that the step does not specify or limit "a logic signal" enough to be a positive and definite limitation to the method step. The examiner suggests a phrase such as "a/the logic 1 [control] signal".

The phrase "transmitting an inverted bit of the first scan data bit from the first SRL to the logic unit", at line 9 (examiner has underlined for emphasis) is not supported

by the hardware, in that the examiner is not sure where the bit is inverted. Because the wording indicates that the bit is inverted at the output of the first SRL, and since there is no support in the Disclosure and Drawings, the phrase is indefinite.

The phrase "the inverted bit" in line 25 is indefinite in view of several references (lines 9, 11, 13 and 18) to an inverted bit. The examiner is unsure to which step/line is being referred.

The phrase "the third SRL" in line 27 is indefinite in that the examiner is unsure if the quoted SRL is the same SRL as "a third SRL" in line 20 or in line 24.

As per Claim 7:

The phrase "the inverted bit" in line 3 is indefinite in view of several references (lines 9, 11, 13 and 18) to an inverted bit in Claim 6. The examiner is unsure to which step/line is being referred.

The phrase "logic 1 signal" in line 4 is indefinite in that the step does not specify or limit "a logic signal" enough to be a positive and definite limitation to the method step. The examiner suggests a phrase such as "the logic 1 [control] signal".

As per Claims 10 and 11:

The phrase "logic 1 signal" in line 5 is indefinite in that the step does not specify or limit "a logic signal" enough to be a positive and definite limitation to the method step. The examiner suggests a phrase such as "the logic 1 [control] signal".

Claim Rejections - 35 USC § 103

1. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Savir, U.S.; Patent No. 5642362, in view of "Scan Latch Design for Delay Test", Jacob Savir, 1997 Test Conference (IEEE Proceedings International), Nov 1-6 1997, pp 446-453, and further in view of Song et al., U.S. Patent No. 6490702.

As per Claim 1:

Savir (5642362) teaches a logic circuit (column 9 line 3) comprising: a combinatorial logic (FIG.4 22) having at least first and second input signal lines (column 9 line 4) and at least a first output signal line (column 9 lines 4-5); and first (FIG.3 1), second (FIG.3 2), and third (FIG.3 18) shift register latches (SRLs) connected to the combinatorial logic (see FIG.3), the third SRL being connected to the first output signal line (FIG.3 OUT) for receiving a first output signal of the combinatorial logic. But Savir (5642362) fails to further teach the exact circuit connections as claimed by the applicant. But in an analogous art, Savir (IEEE Proceedings) does teach the first SRL being connected to the first input signal line for outputting a first scan signal thereto (see page 451 2nd column operation "3."), the second SRL being connected to the second input signal line for outputting a second scan signal thereto (see page 451 2nd column operation "3."); and a logic unit having at least first and second logic input lines (FIG.7b Scan Out with Feedback line) and a logic output line (FIG.7b Scan In), the first logic input line being connected to the first SRL for receiving the first scan signal therefrom (page 450 column 2 last paragraph), the second logic input line being connected to a pattern adjust line for receiving a control signal (FIG.7b Feedback line), the logic output line being connected to the second SRL for outputting a logic output signal thereto

(page 450 column 2 last paragraph), wherein the logic output signal is at least one of the first scan signal and an inverted signal of the first scan signal, depending on the logic value of the control signal (see logic in FIG.7b, which is an XOR inverting array). And Savir (IEEE) on pages 452 and 453 states the advantage as enabling faster AC testing in a distributed manner and not requiring special positioning of logic and latches. One with ordinary skill in the art at the time of the invention, motivated as suggested by Savir (IEEE) would find it obvious to combine the XOR circuit at the scan out and scan in of Savir (IEEE) with the AC test circuit of Savir (5642362), thus providing a better AC test circuit as described. However, neither of the Savir references "suggest employing an SRL latch chain in combination with all other limitations", and where "neither explicitly discloses a chain wherein logic interposed between at least some of the latches" (see page 8, 1st paragraph of amendment). However, Song et al. does teach the amended limitations in the Abstract ("a first shift register latch and a second shift register latch") where a multiplexer logic circuit is placed between the two SRLs for the purpose of inverting the first SRL output and providing the inverted signal to the second SRL. Figure 10 of Song et al. provides the teaching also, where the first SRL (FIG.10 32a/34a) output (FIG.10 114) is inverted or directly applied to the second SRL (FIG.10 32b/34b) through logic (FIG.10 116, 112a) which is under control of a select bit (FIG.10 SEL=0 120). And Song et al., in column 2 lines 61-67 and column 3 lines 1-12, cites the advantage as being a novel way of testing a two-input AND gate between two SRL chain cells at high speed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it to be obvious to add Song et al. logic

between two adjacent scan chain cells in order to test this heretofore untestable condition at high speed.

As per Claim 2:

Savir (IEEE) further teaches the logic circuit of claim 1, wherein the logic unit comprises an XOR gate having the first and second logic input lines and the logic output line (see logic in FIG.7b, which is an XOR inverting array). And in view of the motivation previously mentioned, the claim is rejected.

As per Claim 3:

Savir (IEEE) further teaches the logic circuit of claim 1, wherein the logic output signal is the first scan signal when the control signal is a logical 0, and is the inverted signal when the control signal is a logical 1(see logic in FIG.7b, which is an XOR inverting array). And in view of the motivation previously mentioned, the claim is rejected.

As per Claim 4:

Savir (IEEE) further teaches the logic circuit of claim 1, wherein each of the SRLs comprises a master latch and a slave latch, the slave latch being connected to the master latch for receiving a master output signal therefrom, the master latch having a data input signal line, a scan input signal line, a data clock line, and a scan clock line, the slave latch having a slave clock line (see example Icon 3 SRL in FIG. 9). And in view of the motivation previously mentioned, the claim is rejected.

As per Claim 5:

Savir (IEEE) further teaches the logic circuit of claim 1, wherein each of the first, second, and third SRLs comprises a master latch and a slave latch, the slave latch being connected to the master latch for receiving a master output signal therefrom, the master latch having a data input signal line, a scan input signal line, a data clock line, and a scan clock line, the slave latch having a slave clock line, wherein the master latch is synchronized to a data clock signal on the data clock line for receiving and temporarily storing a logic data bit through the data input signal line, wherein the master latch is synchronized to a scan clock signal on the scan clock line for receiving and temporarily storing a scan data bit through the scan input signal line, and wherein the slave latch is synchronized to a slave clock signal on the slave clock line for receiving and temporarily storing at least one of the logic data bit and the scan data bit from the master latch (see example Icon 3 SRL in FIG. 9). And in view of the motivation previously mentioned, the claim is rejected.

As per Claims 6, 10 and 11:

Savir (5642362) teaches a method and means for enhancing test coverage in a level-sensitive scan design (LSSD) (column 11 line 34), the method comprising the steps of: receiving a first scan data bit by a first SRL (FIG.3 16); temporarily storing the first scan data bit in the first SRL (FIG.3 1 after 1st clock); transmitting the first scan data bit from the first SRL to a second SRL (FIG.3 after 2nd clock); temporarily storing the first scan data bit in the second SRL (FIG.3). However, Savir (5642362) is not specific in teaching the balance of the applicant's claim. But in the analogous art of Savir (IEEE), the following is taught; transmitting an inverted bit of the first scan data bit from the first

SRL to the second SRL (Page 451 step 1); temporarily storing the inverted bit in the second SRL (Page 451 step 2); receiving a second scan data bit by the first SRL (Page 451 step 1); temporarily storing the second scan data bit in the first SRL (Page 451 step 2); transmitting the first scan data bit from the second SRL to a combinatorial logic, and the second scan data bit from the first SRL to the combinatorial logic (Page 451 step 3); transmitting the inverted bit from the second SRL to the combinatorial logic, and the second scan data bit from the first SRL to the combinatorial logic (Page 451 step 4); receiving a first output data bit of the combinatorial logic by a third SRL, the first output data bit being output from the combinatorial logic receiving at least the first and second scan data bits; temporarily storing the first output data bit in the third SRL (Page 451 step 5); receiving a second output data bit of the combinatorial logic by a third SRL, the second output data bit being output from the combinatorial logic receiving at least the inverted bit and the second scan data bit; temporarily storing the second output data bit in the third SRL (Page 451 step 6); and enhancing test coverage of the combinatorial logic by obtaining both the first and second output data bits from the third SRL (Page 451 last 3 paragraphs). However, the amendment submitted by the applicant further limits Claims 6 and 10 to transmitting a first SRL bit to a second SRL if a control signal is 0, and transmitting an inverted bit from the first to the second SRL if the control signal is 1. But Song et al. does teach this feature in FIG.10 (see rejection for Claim 1 above for specifics). And in view of the motivation previously mentioned, the claims are rejected.

As per Claim 7:

Savir (IEEE) further teaches the method of claim 6, wherein the step of transmitting an inverted bit of the first scan data bit from the first SRL to a second SRL further comprises the step of inputting a logical 1 to a first input of an XOR gate (FIG.7b Feedback lines), wherein a second input of the XOR gate is connected to the first SRL for receiving the first scan data bit therefrom (FIG.7b Scan Out), and wherein an output of the XOR gate is connected to a scan input of the second SRL (FIG.7b Scan In). And in view of the motivation previously mentioned, the claim is rejected.

As per Claim 8:

Savir (IEEE) further teaches the method of claim 6, wherein each of the first, second, and third SRLs comprises a master latch and a slave latch, the slave latch being connected to the master latch for receiving a master output signal therefrom, the master latch having a data input signal line, a scan input signal line, a data clock line, and a scan clock line, the slave latch having a slave clock line (see example Icon 3 SRL in FIG. 9). And in view of the motivation previously mentioned, the claim is rejected.

As per Claim 9:

Savir (IEEE) further teaches the method of claim 6, wherein each of the first, second, and third SRLs comprises a master latch and a slave latch, the slave latch being connected to the master latch for receiving a master output signal therefrom, the master latch having a data input signal line, a scan input signal line, a data clock line, and a scan clock line, the slave latch having a slave clock line, wherein the master latch is synchronized to a data clock signal on the data clock line for receiving and temporarily storing a logic data bit through the data input signal line, wherein the master

latch is synchronized to a scan clock signal on the scan clock line for receiving and temporarily storing a scan data bit through the scan input signal line, and wherein the slave latch is synchronized to a slave clock signal on the slave clock line for receiving and temporarily storing at least one of the logic data bit and the scan data bit from the master latch (see example Icon 3 SRL in FIG. 9). And in view of the motivation previously mentioned, the claim is rejected.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is (703)

272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
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